IN THE SPECIFICATION:

Please amend paragraph **[0006]** as follows:

[0006] Wafer carriers may alternatively be configured to establish an electrical connection with a multiplicity of semiconductor devices carried upon a wafer or other substrate by contacting one or more common contact locations formed on the wafer or other substrate. For example, it is known in the art to fabricate wafers with each of the semiconductor devices carried thereon in communication with a common ground contact and a common power (V_{CC}) contact, which are also carried upon the wafer. Conventionally, electrical connection of the common ground contact and the common power (V_{CC}) contact of such a wafer to ground and a power (V_{CC}) source, respectively, has been effected by use of clamping mechanisms, such ~~as C-clamps~~ as C-clamps or so-called "alligator clips" with planar conductive plates thereon.

Please amend paragraph **[0008]** as follows:

[0008] While C-clamps contact larger areas of the respective common ground and power (V_{CC}) contacts formed on the active surface of a wafer, as well as larger areas on the backside of the wafer, and apply force to the wafer in a direction substantially normal, or perpendicular, to the plane of the wafer, C-clamps are relatively clumsy and would, therefore, likely increase the chance that a wafer is damaged as C-clamps are secured to their respective contacts. Moreover, when stress testing involves varied temperatures, the expansion of ~~a C-clamp~~ a C-clamp would increase the amount of force applied to the wafer, which could crack or otherwise damage the wafer, as well as semiconductor devices carried upon the wafer. Conversely, contraction of a C-clamp during cooling could result in an inadequate electrical connection between the C-clamp and its corresponding contact.

Please amend paragraph **[0019]** as follows:

[0019] FIG. 3 is a cross-sectional representation taken along ~~line~~ lines 3-3 of FIG. 2;

Please amend paragraph **[0023]** as follows:

[0023] A semiconductor wafer, referred to herein as a substrate 10, which includes a plurality of semiconductor devices 14 carried upon an active surface 11 thereof, is illustrated in FIG. 1. Substrate 10 also includes, on active surface 11, a common ground contact 16 and a common power (V_{CC}) contact 18. Common ground contact 16 and common power (V_{CC}) contact 18 both communicate with a number of different semiconductor devices 14 on substrate 10 by way of respective circuit traces 17, 19 carried upon active surface 11 of substrate 10. Although substrate 10 is illustrated in FIG. 1 as a semiconductor wafer, the hereinafter described electrical connector of the present invention may be used with other substrates, including, without limitation, individual semiconductor dice, full or partial wafers formed of semiconductive material (e.g., silicon, gallium arsenide, iridium phosphide, etc.), and silicon-on-insulator (SOI) substrates, such as silicon-on-glass (SOG), ~~silcon-on-sapphire~~ silicon-on-sapphire (SOS), and silicon-on-ceramic (SOC).

Please amend paragraph **[0028]** as follows:

[0028] In alternative embodiments, the electrically conductive and attractive elements of an electrical connector incorporating teachings of the present invention may be fully or partially combined. As shown in FIG. 3A, an electrical connector 20′ includes a first member 22′ with a combined electrically conductive/attractive element 26′/28′. Combined element 26′/28′ may comprise a matrix material 30′ impregnated with electrically conductive, Z-axis type filaments, or particles 31′, and attractive particles 29′. Upon positioning first member 22′ with combined element 26′/28′ in contact with a common contact 16, 18 ~~(FIG. 1)~~ of a substrate 10, an electrical connection is established between first member 22′ and one or more semiconductor devices 14 (FIG. 1) on substrate 10. Matrix material 30′ may be a relatively soft, pliable material, such as silicone or another elastomer, so as to prevent common contact 16, 18 from being damaged as first member 22′ is positioned thereagainst.

Please amend paragraph **[0038]** as follows:

[0038] As shown in FIG. 4, substrate 10 and electrical connectors 20 secured thereto are placed within a burn-in oven 60. A preferably substantially constant electrical current is then applied to each semiconductor device 14 carried by substrate 10 through electrical connectors 20 and the temperature of burn-in oven 60 is increased. The temperature of burn-in oven 60 may be increased to a substantially steady temperature or may be varied, as is known in stress testing of semiconductor devices. For example, with reference to FIG. 1, when substrate 10 is a wafer including a plurality of semiconductor devices 14, such as dynamic random access memory (DRAM) devices or static random access memory (SRAM) devices and includes common contacts 16, 18 for connection of each semiconductor device 14 on substrate 10 to a ground 50 and a power (V_{CC}) source 52, such as that depicted in FIG. 1, sufficient current (e.g., about 6-10 amps) is applied to contacts 16, 18 of substrate 10 to permit each semiconductor device 14 carried thereby to draw about ~~10mA.~~ 10 mA. In addition, the temperature of burn-in oven 60 may be cycled during the stress testing process. Of course, electrical connectors incorporating teachings of the present invention, as well as methods of the present invention may also be used to facilitate electrical connections in other testing and use applications.